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**REMARKS**

Claims 1-27 are currently pending in the subject application and are presently under consideration. Claims 1, 13 and 25-27 have been amended herein for clarity or to emphasize various novel aspects of the claimed invention – these amendments do not narrow the scope of the claims. A version of all pending claims is presented at pages 2-6.

Favorable consideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

**I. Rejection of Claims 1-15 and 17-26 Under 35 U.S.C. §102(e)**

Claims 1-15 and 17-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by *Le et al.* (US 6,690,602 B1). It is respectfully requested that this rejection be withdrawn for at least the following reason. *Le et al.* does not teach or suggest each and every limitation as recited in the subject claims.

A single prior art reference anticipates a patent claim only if it expressly or inherently describes each and every limitation set forth in the patent claim. *Trintec Industries, Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the ... claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The claimed invention relates to a core-based multi-bit memory having a dual-bit dynamic referencing architecture fabricated on the memory core. In particular, the referencing architecture is placed internal to the chip, that is, with the core circuitry. The referencing architecture provides for two arrays, one array fixed at a certain voltage level and a second array fixed at another voltage level. When a data cell associated with both reference arrays is read, the reference array voltage levels are read and averaged to determine a proper reference voltage. The reference voltage can then be utilized to determine whether a data bit in the associated data cell is programmed or unprogrammed. Specifically, independent claim 1 recites an *architecture...with... a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage*. Independent claims 13, 17, and 24 recite similar limitation(s).

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Le *et al.* does not teach or suggest *arriving at a reference voltage let alone via averaging of reference array values*. Rather, the cited reference discloses a method of cycling dual bit flash memory arrays having a plurality of dual bit flash memory cells. The Le *et al.* method executes an erase procedure upon both a data sector and reference arrays. (See Le *et al.*, col. 6, ln. 9-11). Next, a soft program step is executed to repair any overerased cells, and appropriate reference array cells are programmed. (See Le *et al.*, col. 6, ln. 12-15). Specifically, cells in one reference array are programmed to 10, cells in the other reference array are programmed to 01 (See Le *et al.*, col. 6, ln. 24-26), and both reference arrays are *ready to function as accurate references*. (See Le *et al.*, col. 3, ln. 42-44). Hence, while the cited reference is directed towards a *method of programming cells in reference arrays* (See Le *et al.*, col. 6, ln. 17-19), it is silent towards *arriving at a reference voltage by averaging bit values of reference cells*.

In view of at least the forgoing, it is respectfully submitted that Let *et al.* does not teach or suggest applicants' invention as recited in the subject claims, and withdrawal of the rejection of claims 1-15 and 17-26 is requested.

## **II. Rejection of Claims 16 and 27 Under 35 U.S.C. §103(a)**

Claims 16 and 27 stand rejected under 35 U.S.C. §103(a) as being obvious over Le *et al.* (US 6,690,602 B1) in view of Le *et al.* (U.S. 6,643,177 B1). It is respectfully requested that this rejection be withdrawn for at least the following reason. The subject matter of the cited references and the claimed invention were, at the time the invention was made, subject to an obligation of assignment to Advanced Micro Devices, Inc. Hence, pursuant to 35 U.S.C. §103(c), a rejection under 35 U.S.C. §103(a) based on either or both of these reference is improper. Accordingly, this rejection should be withdrawn.

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**CONCLUSION**

The present application is believed to be in condition for allowance, in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP975US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

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